Fabrication of a Fast Turn-off Transistor by Wafer Bonding

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Introduction: A new class of electronic devices is presently under development for the Navy's Power Electronic Building Blocks program. One of the prime objectives of the program is to devise new power switching devices dubbed Fast Turn-Off transistors or FTO. Faster power switching devices are desirable on Navy platforms for several reasons: First, as switching frequencies increase the physical size and weight of passive components used in power conditioning systems is reduced. Secondly, the higher switching frequencies make it easier to filter harmonics which improves both silent operation of Navy vessels and electrical power quality. Thirdly, the FTO is projected to reduce switching loss by a factor of 3–5 and thereby improve efficiency of power systems. To speed the development of FTOs, NRL has developed a new wafer bonding technology and together with Harris Semiconductor has demonstrated a new power switching device with potential for dramatically improved performance.

The trend in FTO type devices is to integrate active turn-off capability on *both* sides of the transistor, whereas conventional power switching devices have active turn-off on only one side. The benefit of the additional control gate is to reduce device switching time. The conceptual cross-section of one such FTO is shown in Fig. 1. The Double-Side Insulating Gate Bipolar Transistor (D-IGBT) is essentially two conventional single-side IGBTs (S-IGBT) placed back-to-back. This is a symmetric bipolar transistor with metal-oxide-semiconductor (MOS) gates on both sides to control vertical current flow through the device. For this device, the second gate improves turn-off characteristics by shunting the p^+ emitter (Emitter 2) to the n^- drift region (n^- base) and effectively drains injected holes during device turn-off. In the conventional, single-side device only electron flow is terminated and

holes decay through carrier recombination. The fabrication of such a device is complicated by the need for advanced semiconductor processing on the top *and* bottom of the silicon wafer. NRL recognized that the fabrication procedure could be greatly simplified if two identical devices were bonded together to produce the structure in Fig. 1. Further, if the wafer bonding was performed at sufficiently low temperature (<450 °C), then fully fabricated wafers with complete device metallization could be bonded to produce the D-IGBT without compromising the integrity of the contact metal.

Direct Wafer Bonding: Direct wafer bonding for power device fabrication has been in use since the late 1980's, however, in all previous work bonding temperatures exceeded 1000 °C. The very low temperature bonding process developed at NRL utilizes hydrophobic bonding and long duration, low temperature annealing. The hydrophobic silicon surface is prepared by careful cleaning followed by etching of the native oxide in hydrofluoric acid. This process simultaneously terminates the silicon surface dangling bonds with hydrogen and renders the surface inactive to further oxidation. The wafers are then bonded by bringing the polished surfaces into close proximity and initiating contact at the center. At this point the wafers are weakly bonded by a van der Waals-like force. Annealing at elevated temperatures increases the bond strength. It was found the long duration (≥5 hours) anneals at 400 °C produced sufficient bond strength to dice and package the transistors.

Interface Characterization: Beyond mechanical bond strength, the primary issue with direct wafer bonding is carrier transport across the bond interface. Carrier transport can be affected by potential barriers at the interface, which are caused by unintentional dopants and electron and hole traps. Additionally, traps can act as recombination centers, sinking current during device operation. Simple transport across the interface was characterized with the test structure shown in the inset of Fig. 2. The incremental resistance across the bonded interface was characterized as a function of anneal temperature [1]. For anneal temperatures below 800 °C the resistance was low and no potential barriers were detected. At 800 °C, a significant potential barrier was observed which diminished at 1000 °C. This observation is consistent with boron contamination at the interface. Ubiquitous boron in low concentrations

(~10^{10} cm^{-2}) is unavoidable and at low temperatures the contaminant is inactive. At higher temperatures the dopant boron becomes active, producing a p-type inversion layer in the n-type background silicon. At still higher temperatures, the interfacial boron diffuses into the bulk of the wafer reducing the barrier. Further measurements were performed to characterize trap density at the interface. The *bulk* trap density in the region of the interface was found to be less than 10^{12} cm^{-2} with no detectable traps at the interface.

FTO Fabrication: The very low temperature wafer bonding process was adopted to fabricate the D-IGBT shown in Fig. 1 (red line shows location of bonding interface). In this case, fully qualified 125 mm diameter IGBT wafers from Harris Semiconductor were mechanically thinned to ~200 μm and the backsides were rendered atomically smooth by chemical-mechanical polishing. The wafers were cleaned and the backsides were etched in hydrofluoric acid in a spin/spray tool. Devices on the top were aligned to those on the bottom and the wafers were bonded. Low temperature annealing was performed at 400 °C for 5 hours.

The devices were diced and mounted in a custom package with leads to terminals on both sides. Static device characteristics were consistent with those of the individual IGBTs prior to bonding and no degradation due to the bond interface was observed. The forward and reverse blocking voltage exceeded 1400 V. The forward voltage drop, $V_{E,SAT}$, was 6.2 V at 5.75 A, and was consistent with twice the nominal drop at the design current. The impact of the second gate is illustrated in Fig. 3 which shows the output of the switching waveform analyzer. The emitter current is ramped up through a series inductor by applying a pulse to Gate 1 ($V_{G,1}$). After the current reaches the design value, device is turned off by shorting Gate 1, after which the emitter voltage ($V_{E,1}$) is restored to the supply voltage (600 V). The switching loss is defined as the time that both the emitter current and voltage are present at device terminals. In Fig. 3, the case where Gate 2 ($V_{G,2}$) remains off (S-IGBT operation) is compared to that where Gate 2 is switched on while Gate 1 is switched off (D-IGBT operation). It was found that by turning on Gate 2 *prior* to turning off Gate 1, a clear decrease in turn-off time and switching energy is observed. Gate 2 acts to short the n^- drift region to the bottom p^+ emitter (Emitter 2) and reduce the hole concentration prior to

switching off the device. It was found experimentally that a delay of 6 μs produced a 50% reduction in switching energy (5.5 mJ to 2.7 mJ) at an emitter current and voltage of 5 A and 600 V, respectively. The emitter current fall time dropped from ~1200 ns to ~400 ns.

Significance: A new type of power switching device that will significantly impact many Navy power conditions systems has been demonstrated. Through the use of a novel direct wafer bonding technique developed at NRL, an advanced fast turn-off power switching transistor was realized for the first time. This demonstration indicates that the FTO indeed improves switching performance, and through standard device optimization the full performance gain should be realized.

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(Sponsored by ONR)

References

[1] F.J. Kub, K.D. Hobart and C.A. Desmond, "Electrical Characteristics of Low Temperature Direct Silicon-Silicon Bonding for Power Device Applications," Proc. of the Electrochem. Soc., vol 97-36, p. 466 (1998).

Figures:

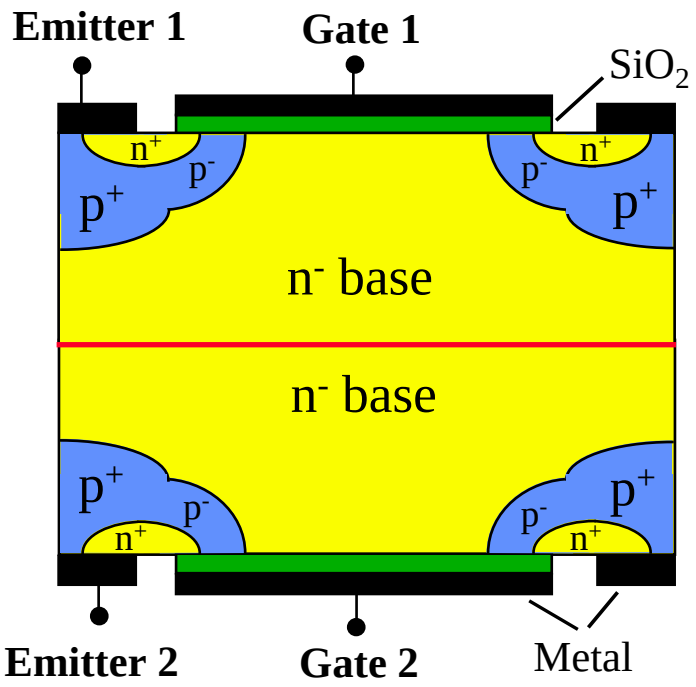

Fig. 1. Schematic cross section of the Double-Side Insulating Gate Bipolar Transistor.

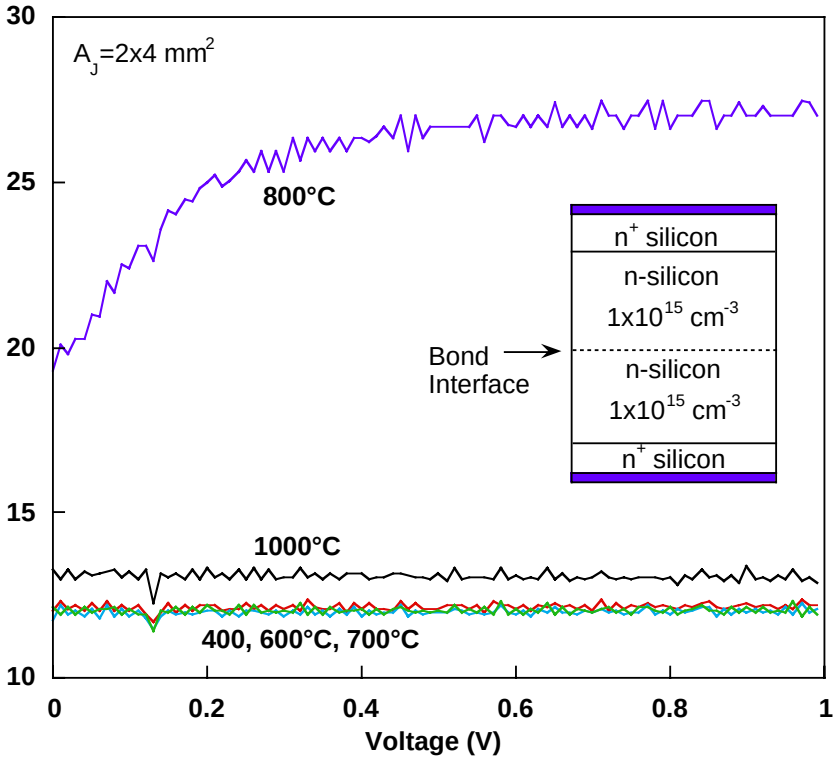

Fig. 2. Incremental resistance vs. bias as a function of anneal temperature of a n-n bonded junction. Non-linear characteristics are evident at 800°C and diminish at 1000°C.

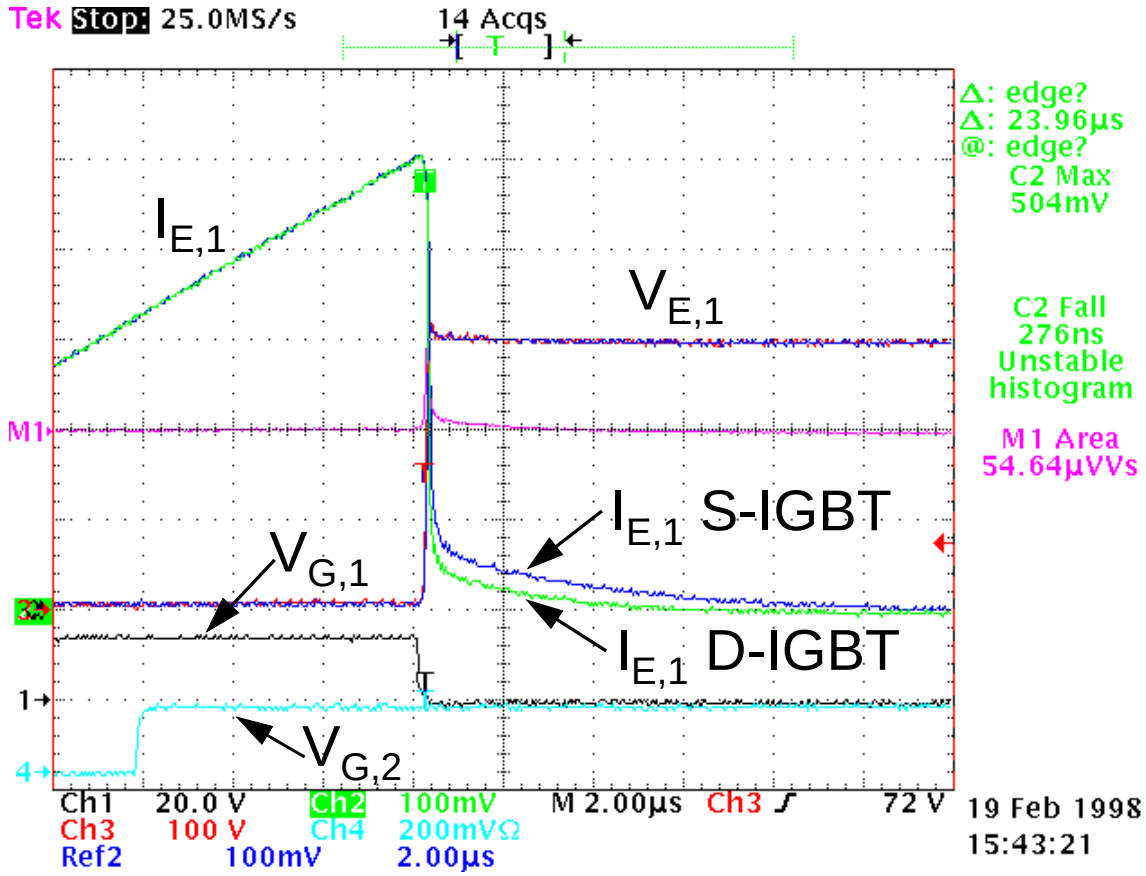

Fig. 3. Switching waveform showing turn-off time of double-side IGBT for two cases (1) Gate 2 (V_{G2}) always off and Gate 1 (V_{G1}) switched off (S-IGBT) and (2) Gate 2 switched on 6 µs prior to switching Gate 1 off (D-IGBT). The emitter voltage and current were 600 V and 5 A, respectively.